ABSTRACT OF THE DISCLOSURE:

A non-volatile semiconductor memory device having a write mode in which wrong writing is prevented surely. The storage device comprises a NAND cell comprising a plurality of memory transistors connected in series and also connected at one end via a select gate transistor CG1 to a bit line BL and at the other end via a select gate transistor SG2 to a common source line SL. A write voltage Vpgm is applied to a control gate of a selected memory transistor in the NAND cell and Vss is applied to the controls gates of non-select memory transistors each adjacent to the selected memory transistor to thereby write data into the select memory transistor. When a second memory transistor from the bit line BL side is selected in the writing operation, a medium voltage Vpass is applied to the control gate of a first non-selected memory transistor from the bit line BL side, and a medium voltage Vpass is applied to the control gates of third and subsequent non-selected memory transistors from the bit line BL side.